Claim 1. (Original) 1. A method of fabricating a capacitor structure for a dynamic random access memory (DRAM), device, on a semiconductor substrate, comprising the steps of:

providing a transfer gate transistor on said semiconductor substrate, comprised of a gate structure on an underlying gate insulator layer, and comprised with a source/drain region located in an area of said semiconductor substrate not covered by said gate structure;

forming a conductive plug structure in an opening in an insulator layer, with said conductive plug structure overlying and contacting a portion of a top surface of a source region;

depositing an intrinsic polysilicon layer on the top surface of said insulator layer, and on the top surface of said conductive plug structure;

performing a series of ion implantation procedures at various implantation energies, to create ion implanted veins at different depths in said intrinsic polysilicon layer, with regions of said intrinsic polysilicon layer located between said ion implanted veins remaining as intrinsic polysilicon regions;

performing a dry etch procedure to define a storage node structure from said intrinsic polysilicon layer, with an isotropic component of said dry etch procedure selectively etching lateral grooves in said ion implanted veins, resulting in a necked profile, storage node structure featuring said lateral grooves in the sides of said necked profile, storage node structure;

forming a capacitor dielectric layer on said necked profile, storage node structure; and

forming an upper electrode structure on said capacitor dielectric layer resulting in said capacitor structure comprised of said upper electrode structure, of said capacitor dielectric layer, and of underlying, said necked profile, storage node structure.

Claims 2 - 27 (cancelled)

Claim 28. (new) A capacitor structure comprising:

a storage node shape with a first portion of said storage node shape overlying a conductive via structure, wherein said storage node shape is located in an opening in an insulator layer, and wherein said conductive via structure contacts a source/drain region of an underlying metal oxide semiconductor field effect transistor (MOSFET), and wherein a second portion of said storage node shape overlying portions of a top surface of said insulator layer;

alternate rows of doped regions in said storage node shape aligned horizontally and parallel to the top surface of said insulator layer, and alternate rows of undoped regions in said storage node shape also aligned horizontally and parallel to the top surface of said insulator layer, with each set of doped regions separated by and undoped region;

lateral grooves extending inwards from sides of each doped region in said storage node shape, and wherein each undoped region of said storage node shape exhibits smooth, non-groove sides;

a capacitor dielectric layer located on a smooth top surface of, and on sides of said storage node shape, and wherein said capacitor dielectric layer contours the surfaces of the lateral grooves in each doped region of said storage node shape; and

a conductive upper node structure located overlying said capacitor dielectric layer.

Claim 29. (new) The capacitor structure of Claim 28, wherein said storage node shape is comprised of polysilicon.

Claim 30. (new) The capacitor structure of Claim 28, wherein the number of said alternate rows of doped regions is between about 3 to 10.

Claim 31.(new) The capacitor structure of Claim 28, wherein each doped region is doped with arsenic or phosphorous ions.

Claim 32. (new) The capacitor structure of Claim 28, wherein the space between doped regions, or the width of each undoped region, is between about 100 to 5000 Angstroms.

Claim 33. (new) The capacitor structure of Claim 28, wherein each lateral groove in each doped region extends inward from the sides of said storage node structure a distance between about 50 to 500 Angstroms.

Claim 34. (new) The capacitor structure of Claim 28, wherein said capacitor dielectric layer is comprised of tantalum oxide, at a thickness between about 10 to 500 Angstroms.

Claim 35. (new) The capacitor structure of Claim 28, wherein said conductive upper node structure is comprised of polysilicon.